

Docket No.: 57454-011

*Image*  
*AF # 2816*  
PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of

Akira YAMAZAKI, et al.

Serial No.: 09/780,477

Filed: February 12, 2001



Customer Number: 20277

Confirmation Number: 6387

Group Art Unit: 2816

Examiner: TRA, Anh Quan

For: MULTI-POWER SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

**TRANSMITTAL OF APPEAL BRIEF**

Mail Stop Appeal Brief - Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellants' Appeal Brief in support of the Notice of Appeal filed November 20, 2003. Please charge the Appeal Brief fee of \$330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

A handwritten signature in cursive script, appearing to read "David M. Tennant".

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**APPEAL BRIEF**

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Commissioner for Patents  
P.O. Box 1450  
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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed November 20, 2003.

**I. REAL PARTY IN INTEREST**

The real party in interest is Renesas Technology Corp.

**II. RELATED APPEALS AND INTERFERENCES**

Appellant is unaware of any related Appeal or Interference.

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### **III.STATUS OF CLAIMS**

Claims 1 through 24 are pending in this application of which claims 1, 11, 19 and 20 are independent. Claims 1 through 24 have been finally rejected. It is from the final rejection of claims 1 through 24 that this appeal is taken.

### **IV.STATUS OF AMENDMENTS**

No Amendment has been filed subsequent to the issuance of the August 20, 2003 Final Office Action.

### **V. SUMMARY OF INVENTION**

The present invention relates to a multi-power semiconductor integrated device and, more particularly, to a multi-power semiconductor integrated circuit device in which a logic circuit and a memory are integrated on the same chip. The present invention addresses and solves the problem of high current consumption when internal circuitry changes states by preventing internal circuits from entering an uncertain state when power is supplied. This is accomplished by maintaining the circuit in a state until the power supply voltages become stable. Advantageously, uncertain states of the internal circuitry can be avoided.

Conventionally, as in Fig. 16 of the Application, an internal voltage generation circuit IVG receiving an external power supply voltage VDDH generates internal power supply voltages VDDS, VPP and VDDP therefrom. Fig. 17 schematically illustrates a power supply structure for a LSI system. As illustrated, logic LG receives a dedicated power supply voltage VDDL applied externally. However, when the logic power supply voltage VDDL is generated by down-converting the external power supply voltage VDDH for DRAM, an ineffective power in a

down-converting circuit is increased to increase power consumption. Therefore, the power supply voltage VDDL for the logic circuit LG is applied from an external source. Accordingly, as Fig. 17 illustrates, two power sources, the external power supply voltage VDDH for DRAM and the power supply voltage VDDL for logic, are used. (*See specification, page 2, line 29 through page 3, line 19*). Consequently, in the conventional LSI system using two power supply voltages applied externally, undesirable through-current associated with the power-up sequence of VDDL and VDDH results. The present invention is made to solve such a through-current problem.

In accordance with the embodiments of the present invention, power supply voltages VDDL and VDDH are applied externally from two power supply sources, and a power-on detectors receiving power supply voltages VDDL and VDDH, respectively, activates power-on detection signals in the claimed manner to solve through-current problems mentioned above.

## VI. ISSUES

### A. The Rejection

1. Claims 1-24 stand finally rejected under 35 U.S.C. §112, first paragraph, for lack of enabling support in the specification.
2. Claims 1-24 stand finally rejected under 35 U.S.C. §112, second paragraph, as being indefinite.
3. Claims 1-3, 7, 19, 21 and 23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Crotty (U.S. Patent No. 6, 160,431).

4. Claims 11, 16-18, 20, 22 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Crotty.

**B. The Issues**

1. Whether claims 1 through 24 are unpatentable under the first paragraph of 35 U.S.C. § 112 for lack of enabling support in the specification;

2. Whether claims 1 through 24 are unpatentable under the second paragraph of 35 U.S.C. § 112 as being indefinite;

3. Whether claims 1-3, 7, 19, 21 and 23 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by Crotty; and

4. Whether claims 11, 16-18, 20, 22 and 24 are unpatentable under 35 U.S.C. § 103(a) for being obvious over Crotty.

**VII. GROUPING OF CLAIMS**

The appealed claims stand or fall together as a group when addressing issues 1 and 2 noted above. Claims 1, 2, 3, 7 and 21 stand or fall together as a group, and claims 19 and 23 stand or fall together as a group when addressing issue number 3 noted above. Claims 11, 16, 17, 18 and 22 stand or fall together as a group, and claims 20 and 24 stand or fall together as a group when addressing issue number 4 noted above.

**VIII. THE ARGUMENT**

**A. The Rejection under the first paragraph of 35 U.S.C. § 112.**

Language at issue can be found in claim 1, which recites “a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power

supply voltage *independently of a voltage level of said first power supply voltage*, to activate a second power-on detection signal according to a result of detection, *said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage.*" Similar language relating to *independently performing detection* can be found in claims 11, 19 and 20 as well, reproduced below.

Claim 11 recites "a power-on detection circuit for detecting power-on of a second power supply voltage *independently of a voltage level of said internal voltage*, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage *independently of a voltage level of the second power supply voltage.*"

Also, claim 19 recites "each power-up detection circuit detecting a voltage level of a corresponding power supply voltage *independently of a voltage level of the power supply voltage other than the corresponding power supply voltage.*"

Even further, claim 20 recites "power-on detection circuitry..., for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage *independently of the voltage level of said at least one internal voltage*,..., said internal voltage power-up detection circuitry performing detection *independently of the voltage level of the at least one power source voltage.*"

The Examiner's rejection under the first paragraph of 35 U.S.C. § 112 is predicated upon the theory that in the specification certain claimed subject matter is not described in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the Application was filed, had possession of the claimed invention. More particularly, the Examiner alleges that the specification fails to teach that the second power-on detection circuit performs a

detection of power-on *independently of the voltage level of the first power supply voltage*, and the specification fails to teach that the first power-on detection circuit performs detection of power-on *independently of the voltage level of the second power supply voltage*. (See *Final Office Action*, page 2). The Examiner alleges further that “it has been well known in the art that a power supply voltage can be generated by another power supply voltage by using a voltage step down circuit or a voltage boosting circuit.” “Therefore, one skilled in the art will not [be] sure that VDDL and VDDH are independent from each other unless the specification clearly teach[es] so.” The Examiner maintains that “claims 1-24 are non-enabled because the specification fails to teach [that] VDDH and VDDL are independent from each other.” Applicants disagree.

Commencing on page 1 of the written description of the specification, line 13, Appellant discloses a conventional general-purpose Dynamic Random Access Memory (DRAM) corresponding to that illustrated by Fig. 16. Therein it is described and illustrated by corresponding Figure(s) that an internal voltage generation circuit IVG receives an external power supply voltage VDDH for generating various internal power supply voltages for internal circuitry of the DRAM. Adverting to page 2 of the written description of the specification, line 21, and referring to Fig. 17, it is described that LSI systems have been widely used in which logic circuits and DRAMs, such as that illustrated by Fig. 16, are integrated on the same semiconductor substrate, such as that schematically illustrated by Fig. 17. It is further disclosed on page 4, lines 6-10, “[w]hen the logic power supply voltage VDDL is generated by down-converting the external power supply voltage VDDH for DRAM, an ineffective power in a down-converting circuit is increased to increase power consumption.” “Therefore, the power supply voltage VDDL for the logic LG is applied from an external source.” Thus, as Fig. 17 illustrates and is supported on page 3, lines 17-19, “two power sources, the external power

supply voltage VDDH for DRAM and the power supply voltage VDDL for logic, are used.” “However, when using two power supply sources, the power supply voltage VDDL for logic and the power supply voltage VDDH for DRAM, the sequence of power-on and a voltage rise time (a time required for entering a settled state) of these power supply voltages VDDL and VDDH are not defined by specifications.” (*See specification, page 4, lines 25-29*). Fig. 19 is a diagram showing an example of voltage generation sequence deficiencies using two power supply sources VDDH and VDDL. It is these problems which the present invention, using two power supply sources, intends to overcome.

Commencing at page 8 of the specification, line 17, it is described a semiconductor integrated circuit in which external power supply voltage VDDL is applied to logic LG and control circuit CTL and external power supply voltage VDDH is applied for the DRAM. This is consistent with the disclosure under the “background of the invention” of the specification. Fig. 17 illustrating a semiconductor integrated circuit device receiving two power supply voltages VDDH and VDDL from two external power supply sources, is equivalently illustrated by Fig. 1. However, also illustrated by Fig. 1 is two independent power-on detectors 10, 11 and a main power-on detection circuit 12 incorporated on the device 1. This solves the problems discussed above when using two external power supply voltage sources. Further discussion of the power supply sources was submitted with the Response filed on June 25, 2003 on pages 11 through 13.

Commencing on page 9 of the written description of the specification, lines 16-31, is found the following description.

The power-on detector 2 includes a power-on detection circuit 10 for detecting power-on of the logic power supply voltage VDDL and holding a power-on detection signal (power-on reset signal) /PORL at an active state while the logic power supply voltage VDDL is unstable (L level), a power-on detection circuit 11 coupled to receive the DRAM power supply voltage VDDH for holding, at the power-on of the DRAM power supply voltage VDDH, a power-on detection signal

(power-on reset signal) /PORH at the active state (L level) until the power supply voltage VDDH becomes stable, and a main power-on detection circuit 12 responsive to these power-on detection signals /PORL and /PORH for maintaining a main power-on detection signal /POROH at the active state (L level) when at least one of the power-on detection signals is active. The main power-on detection signal /POROH from the main power-on detection circuit 12 is applied to the row decoder RD, the write driver WD and others in the DRAM macro DM. In other words, the main power-on detection signal /POROH is applied to a circuit part having the level conversion function.

It is clear that the specification states that each of the power-on detectors 10, 11 detect power-on of the respective DRAM power supply voltage each applied from an independent power supply source. Fig. 1 illustrates power-on detector 10 receiving power supply voltage VDDL for detecting power-on and outputting power-on detection signal /PORL, and power-on detector 11 receiving power supply voltage VDDH and outputting power-on detection signal /PORH. Thus, it may be said that there is no influence of power supply voltage VDDH on power-on detection circuit 10, and no influence of power supply voltage VDDL on power-on detection circuit 11. In other words, the power-on detection circuits 10 and 11 each detect VDDH and VDDL, respectively, without influence of the other power supply. This can also be seen from Figs. 4 and 5 of the application. In these Figures, at power-on of VDDH, power-on detection circuit 10 outputs /PORH, which is fixed at the “L” level, until VDDH attains a stable state. At this time (Tb in Fig. 4), power-on detection circuit 10 outputs /PORH immediately rising to the “H” level. Similarly, at power-on of VDDL, power-on detection circuit 11 outputs a /PORL, which is fixed at the “L” level, until VDDL attains a stable state. At this time (Td in Fig. 4), power-on detection circuit 11 outputs /PORL immediately rising to the “H” level. At power-on of VDDL, there is no influence on the other power on detection circuit 10, as shown by a stable “H” level. Also, in Fig. 5, at power-on of VDDH, there is no influence on the other power-on detection circuit 11, as shown by the stable “H” level.

In accordance with the above disclosure and exemplification, there is explicit support for “a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage *independently of a voltage level of said first power supply voltage, ..., said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage,*” as claim 1 recites. Also clearly supported is the language of claims 11, 19 and 20, which are recited above but not repeated for conciseness.

Bearing in mind the above disclosure and exemplification, there are four relevant legal principles with which the Examiner must consider.

**1. The written description of a patent specification must be presumed enabling.**

*In re Brana*, 51 F.3d 1560, 34 USPQ2d 1436 (Fed. Cir. 1995); *In re Marzocchi*, 439 F.2d 220, 169 USPQ 367 (CCPA 1971).

**2. The burden is on the Examiner.**

When faced with a presumptively enabling disclosure, the Examiner must provide facts or cogent technical reasoning to overcome the legal presumption that one having ordinary skill in the art would have been able to practice the claimed invention, armed with the supporting specification, without **undue experimentation**. *In re Brana, supra.*; *In re Marzocchi, supra.*

The written description of this patent specification is to be presumed enabling. However, the Examiner being faced with the burden of presenting cogent technical reasoning to overcome this legal presumption has failed to provide evidence and support of why his contention would be correct. Moreover, the Examiner has held Appellants to a high burden, by asserting that the specification must “clearly teach” in order to be enabling. According to Section 11 commencing on page 7 of the Final Office Action, the Examiner relies on his position that the specification

must “clearly teach” all aspects of the claim to satisfy the enablement requirement. However, this contention is contrary to legal tenets. Rather, one of ordinary skill in the art armed with the specification must have been able to practice the claimed invention without undue experimentation.

**3. The scope of enablement varies inversely with the degree of predictability in the art.** *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); *U.S. v. Teletronics, Inc.*, 857 F.2d 778 USPQ2d 1217 (Fed. Cir. 1998). The technology involved in practicing the claimed invention does not flirt with the fringes of human ken. Rather, the technology involves detecting a first power supply voltage level of the second power supply voltage and detecting a second power supply voltage independently of a first power supply voltage..

**4. Some experimentation does not trigger lack of enablement.**

While the Examiner appears to be of the opinion that the specification must “clearly teach” (See Final Office Action, page 8, lines 1-2) to satisfy enablement, this is not the law, as the first paragraph of 35 U.S.C. §112 contemplates experimentation. *See, e.g., In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Indeed, given the relatively high degree of disclosure of using two power sources (described above), it is difficult to conceive of one having ordinary skill in the art who would have been hamstrung and unable to practice the claimed invention, again bearing in mind that the specification is presumed enabling. Nevertheless, Appellants submit that the specification does “clearly teach” the disputed claim terminology of claims 1, 11, 19, and 20. At the very least, only minimal experimentation may be needed.

Appellant would again refer to page 3 of the specification where it is described that use of a down-converting circuit increases power consumption. In order to overcome this problem, the

LSI system, as illustrated in Fig. 17, the use of two external power supply sources to generate external power supply voltages VDDH and VDDL has been employed. These independently generated power supply voltages are used in the embodiments described throughout the Application, as we have described above. Thus, the written description does “clearly teach” that “two power sources, the external power supply voltage VDDH for DRAM and the power supply voltage VDDL for logic, are used.” (*See, page 3, lines 17-19*).

Armed with this knowledge, one of ordinary skill in the art reviewing the embodiments disclosed in the application would readily understand that each power-on detector 11, 12 detects power-on of a respective independent power supply received. This is clearly illustrated by at least Fig. 1 and the corresponding timing diagrams of Figs. 4 and 5.

In Section 11, on page 7, of the Final Office Action, the Examiner states even further that “it has been known in the art that a power supply voltage can be generated by another power supply voltage by using a voltage step down circuit or a voltage boosting circuit.” However, the written description of the specification discredits use of a voltage step down circuit because “[w]hen the logic power supply voltage VDDL is generated by down-converting the external power supply voltage VDDH for DRAM, an ineffective power in a down-converting circuit is increased to increase power consumption.” (*See specification, page 4, lines 6-10*). The written description of the specification accordingly describes the use of “two power sources, the external power supply voltage VDDH for DRAM and the power supply voltage VDDL for logic” to overcome problems inherent to down-conversion. (*See specification, page 3, lines 17-19*). It is this structure in which the claimed subject matter is based, and problems with the use of two sources which the present invention intends to overcome.

The Examiner has not made it clear why one of skill in the art when practicing the present invention would use a voltage step down circuit for generating two power supply voltages when the written description explicitly states and describes undesirable affects of using voltage converting circuitry in this manner. To conclude otherwise would be to presume one skilled in the art would not be able to comprehend what is explicitly stated in the Application. Appellants are aware of no such legal presumption. Indeed, it is difficult to envision anyone having ordinary skill in the art, given the guidance of the present disclosure, would not understand and comprehend to provide two power supply sources which, in turn, enables independent detection of power on levels according to each power supply source.

Appellants, therefore, submit that the imposed rejection of claims 1 through 24 under the first paragraph of 35 U.S.C. § 112, for lack of enabling support is not legally viable.

**B. The rejection of claims 1 through 24 under second paragraph of 35 U.S.C. § 112**

Under the grounds of rejection, the Examiner asserts that the specification fails to show the second power on detection circuit performing detection of the power on independently of the voltage level of the first power supply voltage, and the specification fails to show the first power on detection circuit performing detection of the power on independently of the voltage level of the second power supply voltage. The Examiner further contends that it is not seen where the specification teaches that there is no influence of power supply voltage VDDH on power-on detection circuit, and no influence of power supply voltage VDDL on power-on detection circuit 11.

Indefiniteness under the second paragraph of 35 U.S.C. § 112 is a **question of law**, not form. *Personalized Media Communications LLC v. U.S. International Trade Commission*, 161 F.3d 696, 48 USPQ2d 1880 (Fed. Cir. 1998); *Tillotson, Ltd v. Wlaboro Corp.*, 831 F.2d 1033, 4

*USPQ2d 1450 (Fed. Cir. 1987); Orthokinetics Inc. v. Safety Travel Chairs Inc.*, 806 F.2d 1565, 1 USPQ2d 1081 (Fed. Cir. 1986). Accordingly, in rejecting a claim under the second paragraph of 35 U.S.C. § 112, the Examiner must provide a basis in fact and/or cogent technical reasoning to support the ultimate legal conclusion that one having ordinary skill in the art, with the supporting specification in hand, would not be able to reasonably ascertain the scope of protection defined by a claim. *In re Okuzawa*, 537 F.2d 545, 190 USPQ 464 (CCPA 1976). Significantly, consistent judicial precedents holds that reasonable precision in light of the particular subject matter involved is all that is required by the second paragraph of 35 U.S.C. § 112. *Zoltek Corp. v. United States*, 48 Fed. Cl. 240, 57 USPQ2d 1257 (Fed. Cl. 2000); *Miles Laboratories, Inc. v. Shandon, Inc.*, 997 F.2d 870, 27 USPQ2d 1123 (Fed. Cir. 1993); *North American Vaccine, Inc. v. American Cyanamid Co.*, 7 F.3d 1571, 28 USPQ2d 1333 (Fed. Cir. 1993); *U.S. v. Teletronics Inc.*, *supra*; *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ (Fed. Cir. 1986). Appellant would stress that claims must be interpreted as one having ordinary skill in the art would have interpreted the claims in light of and consistent with the supporting specification. *Zoltek Corp. v. United States*, *supra*; *Miles Laboratories, Inc. v. Shandon, Inc.* *supra*.

As described above there is clear support for the claim language at issue. Namely, it has been described in the written description that two external power supply sources supply power supply voltages VDDH and VDDL, which are received by power on detection circuit 10 and power on detection circuit 11, respectively. Then, as described above, each power-on detector 10, 11 outputs a signal in accordance with detection of power-on of the corresponding power supply voltage. Because separate power-on detection circuitry 10, 11 receive independent voltages VDDL, VDDH, respectively, it is most certainly clearly disclosed that there is no influence of one power on detection circuit on the other.

Appellants, therefore, submit that the imposed rejection of claims 1 through 24 under the first paragraph of 35 U.S.C. § 112, for indefiniteness is not legally viable.

**C. Claims 1-3, 7, 19, 21 and 23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Crotty**

In rejecting the above-identified claims as being anticipated by Crotty, the Examiner does not consider certain limitations of independent claims 1 and 19. More particularly, the Examiner alleges that the specification fails to teach elements recited under the enablement rejection, discussed above, and therefore “the limitation “independently” of the voltage level of the first or second power supply voltage is not given any patentable weight.” (*See Final Office Action, Section 7*). The Examiner further alleges that Crotty identically discloses the other elements of the claims 1 and 19. (*See id.*). The Examiner’s position is not legally viable, and even if so, Crotty fails to identically teach each and every element of claims 1 and 19.

The factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized position of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003); *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002). Moreover, in imposing a rejection under 35 U.S.C. §102 for lack of novelty, the Examiner is charged with the burden of specifically identifying where an applied reference discloses each and every feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).

That burden has not been discharged. It is not apparent and the Examiner has failed to specifically identify where Crotty discloses or suggests a semiconductor device including

detectors for *independently performing detection*. This is not a matter of interpreting claims broadly. This is a matter of the Examiner choosing to ignore express claim limitations, *i.e.*, as the Examiner states “the limitation ‘independently’ of the voltage level of the first or second power supply voltage is not given any patentable weight.” (*See Final Office Action, Section 7, paragraph 2*). The Examiner has failed to meet his burden for lack of novelty (explicitly acknowledged by the Examiner) by specifically identifying where an applied reference discloses each and every feature of a claimed invention. There is no known legal precedent permitting an Examiner to ignore claim limitations just because he believes that the claim limitations are not supported by the written description.

There are significant fundamental differences between the claimed inventions and the device disclosed by Crotty that undermines the Examiner’s factual determination that Crotty discloses a semiconductor device identically corresponding to that claimed. These fundamental differences are discussed further below.

Contrary to the teachings of Crotty, claims 1 and 19 require detecting power-on (or a voltage level) independently of another voltage level. Portions of claims 1 and 19 have been reproduced again (*See supra, Section VIII(A)*) for the Examiner’s convenient reference.

Claim 1 recites “a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage *independently of a voltage level of said first power supply voltage*, to activate a second power-on detection signal according to a result of detection, *said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage.*”

Similar language relating to *independently performing detection* can be found in claims 19 as well, reproduced below. Claim 19 recites “each power-up detection circuit detecting a

voltage level of a corresponding power supply voltage *independently of a voltage level of the power supply voltage other than the corresponding power supply voltage.*"

Crotty does not disclose the elements recited above. Crotty discloses in Fig. 6 a power-on detection circuit including dual voltage detection circuit 210 for generating a first voltage level detection signal VD1 having a voltage level determined according to the first power supply voltage Vcc1 *only* when the second power supply voltage Vcc2 is in a steady state. (*Emphasis Added*). This is because the voltage detection signal VD1 is driven by circuitry powered by the second power supply Vcc2, and therefore, must be at a steady state to generate the first voltage level detection signal VD1. (*See Crotty, col. 2, lines 45-55*). A second voltage level detection circuit 630 detects a voltage level of the second power supply voltage Vcc2 to generate the second voltage level detection signal VD2. A buffer circuit 650 receiving signals POR1, POR2 corresponding to VD1 and VD2, respectively, generates the power-on detection signal POR in accordance with voltage level detection signals VD1 and VD2. Consequently, when the second power supply voltage Vcc2 is not supplied (or is at a level below adequate), the first and second power-on detection signals POR1 and POR2 are in an inactive state. (*See col. 9, lines 5-15 and lines 18-24*). Thus, the power-on detection signal POR is also in an inactive state.

In Crotty, detection of Vcc1, the first power supply voltage, is completely dependent on a second power supply voltage, Vcc2. To do otherwise would be contrary to the intended purpose of Crotty because Crotty teaches a dual voltage detector 210 for detecting Vcc1 dependent on a steady level of Vcc2 (*See Crotty, col. 2, lines 45-55*) to overcome the problems of "erroneous results" when a "circuit is partly power up." (*See col. lines 24-31*).

Accordingly, Crotty fails to identically teach "a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply

voltage *independently of a voltage level of said first power supply voltage*, to activate a second power-on detection signal according to a result of detection, *said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage*,” as claim 1 recites; and fails to identically teach "each power-up detection circuit detecting a voltage level of a corresponding power supply voltage *independently of a voltage level of the power supply voltage other than the corresponding power supply voltage*," as claim 19 recites.

Claim 1 further recites “a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.”

Claim 19 further recites “a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.”

As regards the "main power-on detection circuit," the Examiner takes the position that "active" [and "inactive"] are considered the states of a signal... a low state is seen as active state, and a high state is seen as inactive state." (*See Office Action of 03/25/2003, Section 12*). The Examiner states further “[o]ne can define a level of a signal as an ‘active state’ or inactive state depending on his or her preference.” Because the written description of the specification describes a low level signal as an active state, the Examiner states that “a low level of the Power-

On Reset signal (POR1, POR2) [of Crotty] is interpreted as an active state..." (*See Final Office Action, Section 11*). The Examiner interprets the claims in this manner so that Crotty reads on the main power-on detection circuit elements of claims 1 and 19.

More particularly, the Examiner takes this position because buffer circuit 650 (which the Examiner correlates is the claimed main power-on detection circuit) may be an AND gate, and asserts that the AND gate, *while not considering any other factors*, could output a main power-on detection signal in accordance with the claims. This interpretation is contrary to the operation of the actual buffer circuit 650 disclosed by Crotty. On col. 9, lines 20-24, Crotty explicitly states that "[buffer] circuit 650 outputs a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period time." Therefore, in order to employ an AND gate as the buffer, an active state of a Power-On Reset signal (POR1, POR2) must be a high state (and not a low state as asserted by the Examiner) to follow disclosed implementation of the buffer circuit 650. In other words, when any of the supply voltages are less than adequate (supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2), the POR signal must be in a power-off logic level. This output state for an AND gate corresponds to inputs of (0,0), (0,1) and (1,0). To state it another way, when the voltage level of the first power supply voltage Vcc1 is insufficient, the internal circuit receiving the second power supply voltage for operation is reset. Therefore, Crotty is directed to detection of a single power application sequence. Specifically, when the first power supply voltage is applied while the second power supply voltage is not applied, the power on reset signal POR is activated, as shown in Figs. 3(b), 3(d), and Fig. 8 of Crotty.

Following the Examiner's interpretation of Crotty, to employ a power-on reset signal,

rendered active from activation of a first activated power-on detection signal (inputs to AND gate of (1,0) or (1, 0)) of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals (inputs to the AND gate of (0, 0)), would be contrary to the explicit teachings of Crotty using an AND gate as a buffer. In other words, following the Examiner's interpretation, buffer circuit 650 would be incapable of outputting "a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period time," as Crotty requires.

In accordance with the foregoing, Crotty fails to identically disclose each and every element of independent claims 1 and 19. Claims dependent therefrom are patentable at least based on dependency to any one of these claims. Accordingly, the rejection of claims 1-3, 7, 19, 21 and 23 under 35 U.S.C. §102(e) maintained by the Examiner should be withdrawn.

**D. Claims 11, 16-18, 20, 22 and 24 stand rejected under 35 U.S.C. §103(a) as being obvious over Crotty.**

In rejecting the above-identified claims as being obvious over Crotty, the Examiner does not consider certain limitations of independent claims 1 and 20, as in the case of the anticipation rejection discussed above. While the Examiner's position is not legally erroneous, the Crotty combination fails to identically teach each and every element of claims 11 and 20. Appellants submit that the record does not establish obviousness for any of the claims on appeal when considered within the framework of well developed legal precedent, briefly summarized below.

Obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art, *Graham v. John Deere Co.* 383 U.S. 1, 13, 148 USPQ 459, 465 (1966). In making this determination, the PTO is charged

with the initial burden of identifying a source in the applied prior art for: (1) claim features; and (2) the realistic requisite motivation for combining applied references to arrive at the claimed invention with a reasonable expectation of successfully achieving a specific benefit. *Smith Industries Medical Systems v. Vital Signs*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999). Even if the prior art *could* have been modified so as to result in the combination defined by the claims, the modification would not have been obvious unless the prior art suggested the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using appellant's claims as a guide. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). A compelling reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention must be formulated. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Rejections under 35 U.S.C. §103 must be predicated upon facts, not assumptions. *In re Freed*, 425 F.2d 785, 165 USPQ 570 (CCPA 1970); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967); *In re Lunsford*, 357 F.2d 385, 148 USPQ 721 (CCPA 1966). What may or may not be known in general does not establish the requisite realistic motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995). The requisite motivation is not an abstract concept, but must stem from the applied prior art as a whole and have realistically impelled one having ordinary

skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). In consideration of the prior art as a whole, it is impermissible to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *In re Wesslau*, 353 F.2d 241, 147 USPQ 393. The totality of the prior art disclosures must not lead substantially away from the claimed invention. *In re Hedges*, 753 F.2d 781, 228 USPQ2d 685 (Fed. Cir. 1986). Emphasis in a reference of the importance of a feature is a significant factor in determining whether or not it would have been obvious to change the disclosed feature. *In re Bell*, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993).

Adverting to the claims, claim 11 recites "a power-on detection circuit for detecting power-on of a second power supply voltage *independently of a voltage level of said internal voltage*, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage *independently of a voltage level of the second power supply voltage*."

Also, claim 20 recites "power-on detection circuitry..., for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage *independently of the voltage level of said at least one internal voltage*..., said internal voltage power-up detection circuitry performing detection *independently of the voltage level of the at least one power source voltage*."

Repeatedly throughout the Examiner's analysis, the limitations italicized above have been completely ignored, as in the case with the anticipation rejection. In the case of an obviousness

rejection, the Examiner is charged with the initial burden of identifying each and every element in a combination and must provide proper motivation for the combination. By the Examiner choosing to ignore claim limitations that are *italicized* above, the Examiner has failed to discharge this initial burden. Appellants are unaware of any case law precedent which lowers the Examiner's burden of proof for an obviousness rejection when the indefiniteness and lack of support is also alleged.

As in claims 11 and 20, there are significant fundamental differences between the claimed inventions and the device disclosed by Crotty that undermines the Examiner's factual determination that the Crotty combination discloses a semiconductor device identically corresponding to that claimed. These fundamental differences have been discussed above under the anticipation rejection analysis relating to the language found italicized in the claims above, and detailed arguments on this point are not repeated for sake of conciseness.

In summary, Crotty fails to disclose *independent detection* as is required by claim 11 and by claim 20. Crotty also fails to disclose main power detection circuitry (claim 11) or power-on detection circuitry (claim 20).

Specifically, in claim 11, the "main power-on detection signal [is] rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal." Because the signal is "rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal," the buffer circuit 650 of Crotty would be incapable of outputting "a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for

longer than a transient period time,” as is required.

In claim 20, the “main power-on detection signal [is] made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.” Because the signal is “made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal,” the buffer circuit 650 of Crotty would be incapable of outputting “a power-on reset signal POR, which is in the power-off logic level, if supply voltage  $V_{cc1}$  is less than adequate or if supply voltage  $V_{cc2}$  is less than adequate voltage  $V_{ad2}$  for longer than a transient period time,” as is required.

Other issues are apparent in the Examiner’s obviousness analysis are discussed further below.

The Examiner alleges that Fig. 9 of Crotty discloses all of the limitations of claims 11 and 20 except for the internal voltage generation circuit receiving a first power supply and generating an internal voltage.

Col. 9 of Crotty, as the Examiner references, describes the embodiment incorporating voltage detection circuit 630 in parallel with dual-voltage detection circuit 210 of Fig. 2, the output of which is received by a dual-input low pass filter 930. The filter includes an OR gate 950 for removing transient signal levels that the Examiner considers to be analogous with the disclose main power detection circuitry (claim 11) or power-on detection circuitry (claim 20). However, it is buffer circuit 650 of Crotty which outputs the main power signal, and has been distinguished above.

Also, in the Office Action of November 7, 2002, the Examiner acknowledged that Crotty does not disclose internal voltage generation circuits of 11 and 20, but asserts that it would have been obvious to use a voltage step-down circuit. Specifically, the Examiner states that it is well known in the arts that 5 volts is a common voltage level. Because Crotty teaches using 3.3 volts, the Examiner asserts that it would be obvious to use a step down circuit for down-converting a supplied voltage.

On page 13 of the Amendment dated February 7, 2003, Applicants traversed and pointed out to the Examiner that a conclusion of obviousness must be factually supported, evidence must be produced to support such a modification, and motivation must be provided. In the Office Action of March 23, 2003, and in response thereto, the Examiner simply states that "it is notorious well known in the art that a voltage step down circuit is [used]..." However, simply stating that something is "notoriously" well-known does not rise to the level of factual support of a modification. Applicants again seasonably traversed the Examiner's assertion that combination is notoriously well-known in the art, requested that the Examiner produce evidence thereof, and submit proper motivation, as previously requested. In the Final Office Action of August 20, 2003, the Examiner reiterated that use of a voltage step-down circuit is notoriously well known, and but in the responsive arguments (*See Section 11*), U.S. Patent No. 5,457,421 (the '421 patent) has been referenced as one example of a voltage step-down circuit.

However, Appellants again emphasize that motivation must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Simply stating that the '421 patent shows an example of

the voltage step-down circuit without providing some type of motivation gleaned from the references as a whole to modify the invention is not legally viable, and equates to what is generally referred to as “piecemeal examination.” Notwithstanding, the Examiner has failed to meet his burden of proof.

In accordance with the foregoing, Crotty fails to identically disclose each and every element of independent claims 11 and 20. Claims dependent therefrom are patentable at least based on dependency to any one of these claims. Accordingly, the rejection of claims 11, 16-18, 20, 22 and 24 under 35 U.S.C. §103 maintained by the Examiner should be withdrawn.

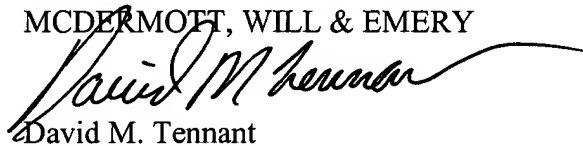
## **IX. CONCLUSION**

Based upon the argument submitted *supra*, Appellants submit that the imposed rejections under the first and second paragraphs of 35 U.S.C. §112 and under 35 U.S.C. §§102 and 103 are erroneous. Appellants, therefore, solicit the Honorable Board to reverse each of the Examiner’s rejections of the appealed claims under the first and second paragraphs of 35 U.S.C. §112 and under 35 U.S.C. §§102 and 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

A handwritten signature in black ink, appearing to read "David M. Tennant", with a long, sweeping horizontal line extending to the right.

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## X. APPENDIX

1. (Previously Presented) A semiconductor integrated circuit device comprising:

a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;

a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage independently of a voltage level of said first power supply voltage, to activate a second power-on detection signal according to a result of detection, said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage;

a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

2. (Original) The semiconductor integrated circuit device according to claim 1, wherein said main power-on detection circuit comprises

a first reset element responsive to activation of said first power-on detection signal for resetting a first node to a first voltage level,

a second reset element responsive to activation of said second power-on detection signal for resetting said first node to said first voltage level, and

a circuit coupled to said first node and receiving said first power supply voltage as an operation power supply voltage for inactivating said main power-on detection signal and setting said first node to a second voltage level when both of said first and second power-on detection signals are inactivated.

3. (Original) The semiconductor integrated circuit device according to claim 1, further comprising a converting voltage application detection circuit receiving a voltage different in voltage level from said second power supply voltage as an operation power supply voltage for converting a voltage level of said main power-on detection signal to generate a converted voltage application detection signal.

4. (Original) The semiconductor integrated circuit device according to claim 1, further comprising:

an internal voltage generation circuit for generating an internal voltage from said first power supply voltage, said internal voltage differing in voltage level from said second power supply voltage; and

an internal circuit reset when said main power-on detection signal is activated, and activated, when said main power-on detection signal is inactivated, for converting a signal having an amplitude of said second power supply voltage level into a signal having an amplitude of the internal voltage level.

5. (Original) The semiconductor integrated circuit device according to claim 4, wherein said internal voltage is a boosted voltage higher in voltage level than said first power

supply voltage.

6. (Original) The semiconductor integrated circuit device according to claim 4, wherein said internal voltage is a down-converted voltage lower in voltage level than said first power supply voltage.

7. (Original) The semiconductor integrated circuit device according to claim 1, wherein the first and second power supply voltages are applied to a storage device and said second power supply voltage is applied to a logic circuit, the storage device and the logic circuit being integrated on a common semiconductor chip.

8. (Original) The semiconductor integrated circuit device according to claim 1, wherein said main power-on detection signal has an amplitude of the first power supply voltage level, and

said semiconductor integrated circuit device further comprises:

an internal voltage generation circuit for generating, from said first power supply voltage, an internal voltage different in voltage level from said second power supply voltage;

an internal signal generation circuit for generating an internal signal having an amplitude of the internal voltage level from a signal having an amplitude of the second power supply voltage level, said internal signal generation circuit including a buffer circuit receiving said internal voltage as an operation power supply voltage for generating said internal signal; and

a converting voltage application detection circuit for converting said main power-on detection signal into a converted voltage application detection signal having an amplitude of said

internal voltage level and applying the converted voltage application detection signal to said buffer circuit, said buffer circuit being reset when said converted voltage application detection signal is activated.

9. (Original) The semiconductor integrated circuit device according to claim 8, wherein said internal voltage generation circuit includes a boosting circuit for boosting said first power supply voltage to generate said internal voltage.

10. (Original) The semiconductor integrated circuit device according to claim 8, wherein said internal voltage generation circuit includes an internal down-converting circuit for down-converting said first power supply voltage to generate an internal power supply voltage as said internal voltage.

11. (Previously Presented) A semiconductor integrated circuit device comprising;  
an internal voltage generation circuit receiving a first power supply voltage and  
generating, from said first power supply voltage, an internal voltage different in voltage level  
from said first power supply voltage;

an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage independently of a voltage level of said internal voltage, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage independently of a voltage level of the

second power supply voltage; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal.

12. (Original) The semiconductor integrated circuit device according to claim 11, further comprising an internal signal generation circuit inactivated when the main power-on detection signal from said main power-on detection circuit is activated, and activated, when said main power-on detection signal is inactivated, for generating an internal signal having an amplitude of said internal voltage level from a signal having an amplitude of said second power supply voltage level.

13. (Original) The semiconductor integrated circuit device according to claim 12, wherein

said internal signal generation circuit includes a buffer circuit receiving said internal voltage as an operation power supply voltage and generating said internal signal, said buffer circuit being reset when said main power-on detection signal is activated and buffering a level converted signal to generate said internal signal when said main power-on detection signal is inactivated.

14. (Original) The semiconductor integrated circuit device according to claim 11, wherein said main power-on detection signal is a signal having an amplitude of said internal voltage level, and

said integrated circuit device further comprises

a level conversion circuit for converting a voltage level of said main power-on detection signal to generate a converted voltage application detection signal, and

an internal signal generation circuit inactivated when said converted voltage application detection signal is activated and activated, when said converted voltage application detection signal is inactivated, for converting a level of a signal having an amplitude of said second power supply voltage level to generate an internal signal having an amplitude equal to an amplitude of said converted voltage application detection signal.

15. (Original) The semiconductor integrated circuit device according to claim 14, further comprising an internal power supply circuit for generating, from said first power supply voltage, an internal power supply voltage different in voltage level from said internal voltage, wherein

said internal signal generation circuit includes a buffer circuit receiving said internal power supply voltage as an operation power supply voltage and buffering a level converted signal for outputting, said buffer circuit having an internal node being reset when said converted voltage application detection signal is activated.

16. (Original) The semiconductor integrated circuit device according to claim 11, wherein said internal voltage generation circuit includes a boosting circuit for boosting said first

power supply voltage.

17. (Original) The semiconductor integrated circuit device according to claim 11, wherein said internal voltage generation circuit includes a down-converting circuit for down-converting said first power supply voltage to generate said first internal voltage.

18. (Original) The semiconductor integrated circuit device according to claim 11, wherein the first and second power supply voltages are applied to a storage device and said second power supply voltage is applied to a logic circuit, said storage device and said logic circuit being integrated on a common semiconductor chip.

19. (Previously Presented) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages, each power-up detection circuit detecting a voltage level of a corresponding power supply voltage independently of a voltage level of the power supply voltage other than the corresponding power supply voltage; and

a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

20. (Previously Presented) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltages differing in voltage level from each other;

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage independently of the voltage level of said at least one internal voltage, to generate at least one power-on detection signal for the respective at least one power source voltage, said internal voltage power-up detection circuitry performing detection independently of the voltage level of the at least one power source voltage; and

main power-on detection circuitry responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.

21. (Previously Presented) The semiconductor integrated device according to claim 1,

wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

22. (Previously Presented) The semiconductor integrated circuit device according to claim 11, wherein activation of the detection signal indicates instability of a corresponding power supply voltage, and inactivation of the detection signal indicates stability of the corresponding power supply voltage.

23. (Previously Presented) The semiconductor device according to claim 19, wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

24. (Previously Presented) The semiconductor device according to claim 20, wherein the activation of the detection signal indicates instability of a corresponding voltage and the inactivation of the detection signal indicates stability of the corresponding voltage.

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Docket No.: 57454-011

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of

Akira YAMAZAKI, et al.

Serial No.: 09/780,477

Filed: February 12, 2001



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Customer Number: 20277

Confirmation Number: 6387

Group Art Unit: 2816

Examiner: Tra, Anh Quan

For: MULTI-POWER SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

**APPEAL BRIEF**

Mail Stop Appeal Brief - Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed November 20, 2003.

**I. REAL PARTY IN INTEREST**

The real party in interest is Renesas Technology Corp.

**II. RELATED APPEALS AND INTERFERENCES**

Appellant is unaware of any related Appeal or Interference.

### III. STATUS OF CLAIMS

Claims 1 through 24 are pending in this application of which claims 1, 11, 19 and 20 are independent. Claims 1 through 24 have been finally rejected. It is from the final rejection of claims 1 through 24 that this appeal is taken.

### IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the issuance of the August 20, 2003 Final Office Action.

### V. SUMMARY OF INVENTION

The present invention relates to a multi-power semiconductor integrated device and, more particularly, to a multi-power semiconductor integrated circuit device in which a logic circuit and a memory are integrated on the same chip. The present invention addresses and solves the problem of high current consumption when internal circuitry changes states by preventing internal circuits from entering an uncertain state when power is supplied. This is accomplished by maintaining the circuit in a state until the power supply voltages become stable. Advantageously, uncertain states of the internal circuitry can be avoided.

Conventionally, as in Fig. 16 of the Application, an internal voltage generation circuit IVG receiving an external power supply voltage VDDH generates internal power supply voltages VDDS, VPP and VDDP therefrom. Fig. 17 schematically illustrates a power supply structure for a LSI system. As illustrated, logic LG receives a dedicated power supply voltage VDDL applied externally. However, when the logic power supply voltage VDDL is generated by down-converting the external power supply voltage VDDH for DRAM, an ineffective power in a

down-converting circuit is increased to increase power consumption. Therefore, the power supply voltage VDDL for the logic circuit LG is applied from an external source. Accordingly, as Fig. 17 illustrates, two power sources, the external power supply voltage VDDH for DRAM and the power supply voltage VDDL for logic, are used. (*See specification, page 2, line 29 through page 3, line 19*). Consequently, in the conventional LSI system using two power supply voltages applied externally, undesirable through-current associated with the power-up sequence of VDDL and VDDH results. The present invention is made to solve such a through-current problem.

In accordance with the embodiments of the present invention, power supply voltages VDDL and VDDH are applied externally from two power supply sources, and a power-on detectors receiving power supply voltages VDDL and VDDH, respectively, activates power-on detection signals in the claimed manner to solve through-current problems mentioned above.

## VI. ISSUES

### A. The Rejection

1. Claims 1-24 stand finally rejected under 35 U.S.C. §112, first paragraph, for lack of enabling support in the specification.
2. Claims 1-24 stand finally rejected under 35 U.S.C. §112, second paragraph, as being indefinite.
3. Claims 1-3, 7, 19, 21 and 23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Crotty (U.S. Patent No. 6, 160,431).

4. Claims 11, 16-18, 20, 22 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Crotty.

**B. The Issues**

1. Whether claims 1 through 24 are unpatentable under the first paragraph of 35 U.S.C. § 112 for lack of enabling support in the specification;

2. Whether claims 1 through 24 are unpatentable under the second paragraph of 35 U.S.C. § 112 as being indefinite;

3. Whether claims 1-3, 7, 19, 21 and 23 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by Crotty; and

4. Whether claims 11, 16-18, 20, 22 and 24 are unpatentable under 35 U.S.C. § 103(a) for being obvious over Crotty.

**VII. GROUPING OF CLAIMS**

The appealed claims stand or fall together as a group when addressing issues 1 and 2 noted above. Claims 1, 2, 3, 7 and 21 stand or fall together as a group, and claims 19 and 23 stand or fall together as a group when addressing issue number 3 noted above. Claims 11, 16, 17, 18 and 22 stand or fall together as a group, and claims 20 and 24 stand or fall together as a group when addressing issue number 4 noted above.

**VIII. THE ARGUMENT**

**A. The Rejection under the first paragraph of 35 U.S.C. § 112.**

Language at issue can be found in claim 1, which recites “a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power

supply voltage *independently of a voltage level of said first power supply voltage*, to activate a second power-on detection signal according to a result of detection, *said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage.*" Similar language relating to *independently performing detection* can be found in claims 11, 19 and 20 as well, reproduced below.

Claim 11 recites "a power-on detection circuit for detecting power-on of a second power supply voltage *independently of a voltage level of said internal voltage*, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage *independently of a voltage level of the second power supply voltage.*"

Also, claim 19 recites "each power-up detection circuit detecting a voltage level of a corresponding power supply voltage *independently of a voltage level of the power supply voltage other than the corresponding power supply voltage.*"

Even further, claim 20 recites "power-on detection circuitry..., for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage *independently of the voltage level of said at least one internal voltage*..., said internal voltage power-up detection circuitry performing detection *independently of the voltage level of the at least one power source voltage.*"

The Examiner's rejection under the first paragraph of 35 U.S.C. § 112 is predicated upon the theory that in the specification certain claimed subject matter is not described in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the Application was filed, had possession of the claimed invention. More particularly, the Examiner alleges that the specification fails to teach that the second power-on detection circuit performs a

detection of power-on *independently of the voltage level of the first power supply voltage*, and the specification fails to teach that the first power-on detection circuit performs detection of power-on *independently of the voltage level of the second power supply voltage*. (See *Final Office Action*, page 2). The Examiner alleges further that “it has been well known in the art that a power supply voltage can be generated by another power supply voltage by using a voltage step down circuit or a voltage boosting circuit.” “Therefore, one skilled in the art will not [be] sure that VDDL and VDDH are independent from each other unless the specification clearly teach[es] so.” The Examiner maintains that “claims 1-24 are non-enabled because the specification fails to teach [that] VDDH and VDDL are independent from each other.” Applicants disagree.

Commencing on page 1 of the written description of the specification, line 13, Appellant discloses a conventional general-purpose Dynamic Random Access Memory (DRAM) corresponding to that illustrated by Fig. 16. Therein it is described and illustrated by corresponding Figure(s) that an internal voltage generation circuit IVG receives an external power supply voltage VDDH for generating various internal power supply voltages for internal circuitry of the DRAM. Adverting to page 2 of the written description of the specification, line 21, and referring to Fig. 17, it is described that LSI systems have been widely used in which logic circuits and DRAMs, such as that illustrated by Fig. 16, are integrated on the same semiconductor substrate, such as that schematically illustrated by Fig. 17. It is further disclosed on page 4, lines 6-10, “[w]hen the logic power supply voltage VDDL is generated by down-converting the external power supply voltage VDDH for DRAM, an ineffective power in a down-converting circuit is increased to increase power consumption.” “Therefore, the power supply voltage VDDL for the logic LG is applied from an external source.” Thus, as Fig. 17 illustrates and is supported on page 3, lines 17-19, “two power sources, the external power

supply voltage VDDH for DRAM and the power supply voltage VDDL for logic, are used.” “However, when using two power supply sources, the power supply voltage VDDL for logic and the power supply voltage VDDH for DRAM, the sequence of power-on and a voltage rise time (a time required for entering a settled state) of these power supply voltages VDDL and VDDH are not defined by specifications.” (*See specification, page 4, lines 25-29*). Fig. 19 is a diagram showing an example of voltage generation sequence deficiencies using two power supply sources VDDH and VDDL. It is these problems which the present invention, using two power supply sources, intends to overcome.

Commencing at page 8 of the specification, line 17, it is described a semiconductor integrated circuit in which external power supply voltage VDDL is applied to logic LG and control circuit CTL and external power supply voltage VDDH is applied for the DRAM. This is consistent with the disclosure under the “background of the invention” of the specification. Fig. 17 illustrating a semiconductor integrated circuit device receiving two power supply voltages VDDH and VDDL from two external power supply sources, is equivalently illustrated by Fig. 1. However, also illustrated by Fig. 1 is two independent power-on detectors 10, 11 and a main power-on detection circuit 12 incorporated on the device 1. This solves the problems discussed above when using two external power supply voltage sources. Further discussion of the power supply sources was submitted with the Response filed on June 25, 2003 on pages 11 through 13.

Commencing on page 9 of the written description of the specification, lines 16-31, is found the following description.

The power-on detector 2 includes a power-on detection circuit 10 for detecting power-on of the logic power supply voltage VDDL and holding a power-on detection signal (power-on reset signal) /PORL at an active state while the logic power supply voltage VDDL is unstable (L level), a power-on detection circuit 11 coupled to receive the DRAM power supply voltage VDDH for holding, at the power-on of the DRAM power supply voltage VDDH, a power-on detection signal

(power-on reset signal) /PORH at the active state (L level) until the power supply voltage VDDH becomes stable, and a main power-on detection circuit 12 responsive to these power-on detection signals /PORL and /PORH for maintaining a main power-on detection signal /POROH at the active state (L level) when at least one of the power-on detection signals is active. The main power-on detection signal /POROH from the main power-on detection circuit 12 is applied to the row decoder RD, the write driver WD and others in the DRAM macro DM. In other words, the main power-on detection signal /POROH is applied to a circuit part having the level conversion function.

It is clear that the specification states that each of the power-on detectors 10, 11 detect power-on of the respective DRAM power supply voltage each applied from an independent power supply source. Fig. 1 illustrates power-on detector 10 receiving power supply voltage VDDL for detecting power-on and outputting power-on detection signal /PORL, and power-on detector 11 receiving power supply voltage VDDH and outputting power-on detection signal /PORH. Thus, it may be said that there is no influence of power supply voltage VDDH on power-on detection circuit 10, and no influence of power supply voltage VDDL on power-on detection circuit 11. In other words, the power-on detection circuits 10 and 11 each detect VDDH and VDDL, respectively, without influence of the other power supply. This can also be seen from Figs. 4 and 5 of the application. In these Figures, at power-on of VDDH, power-on detection circuit 10 outputs /PORH, which is fixed at the “L” level, until VDDH attains a stable state. At this time (Tb in Fig. 4), power-on detection circuit 10 outputs /PORH immediately rising to the “H” level. Similarly, at power-on of VDDL, power-on detection circuit 11 outputs a /PORL, which is fixed at the “L” level, until VDDL attains a stable state. At this time (Td in Fig. 4), power-on detection circuit 11 outputs /PORL immediately rising to the “H” level. At power-on of VDDL, there is no influence on the other power on detection circuit 10, as shown by a stable “H” level. Also, in Fig. 5, at power-on of VDDH, there is no influence on the other power-on detection circuit 11, as shown by the stable “H” level.

In accordance with the above disclosure and exemplification, there is explicit support for “a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage *independently of a voltage level of said first power supply voltage, ..., said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage,*” as claim 1 recites. Also clearly supported is the language of claims 11, 19 and 20, which are recited above but not repeated for conciseness.

Bearing in mind the above disclosure and exemplification, there are four relevant legal principles with which the Examiner must consider.

**1. The written description of a patent specification must be presumed enabling.**

*In re Brana*, 51 F.3d 1560, 34 USPQ2d 1436 (Fed. Cir. 1995); *In re Marzocchi*, 439 F.2d 220, 169 USPQ 367 (CCPA 1971).

**2. The burden is on the Examiner.**

When faced with a presumptively enabling disclosure, the Examiner must provide facts or cogent technical reasoning to overcome the legal presumption that one having ordinary skill in the art would have been able to practice the claimed invention, armed with the supporting specification, without **undue experimentation**. *In re Brana, supra.*; *In re Marzocchi, supra.*

The written description of this patent specification is to be presumed enabling. However, the Examiner being faced with the burden of presenting cogent technical reasoning to overcome this legal presumption has failed to provide evidence and support of why his contention would be correct. Moreover, the Examiner has held Appellants to a high burden, by asserting that the specification must “clearly teach” in order to be enabling. According to Section 11 commencing on page 7 of the Final Office Action, the Examiner relies on his position that the specification

must “clearly teach” all aspects of the claim to satisfy the enablement requirement. However, this contention is contrary to legal tenets. Rather, one of ordinary skill in the art armed with the specification must have been able to practice the claimed invention without undue experimentation.

**3. The scope of enablement varies inversely with the degree of predictability in the art.** *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); *U.S. v. Teletronics, Inc.*, 857 F.2d 778 USPQ2d 1217 (Fed. Cir. 1998). The technology involved in practicing the claimed invention does not flirt with the fringes of human ken. Rather, the technology involves detecting a first power supply voltage level of the second power supply voltage and detecting a second power supply voltage independently of a first power supply voltage..

**4. Some experimentation does not trigger lack of enablement.**

While the Examiner appears to be of the opinion that the specification must “clearly teach” (See Final Office Action, page 8, lines 1-2) to satisfy enablement, this is not the law, as the first paragraph of 35 U.S.C. §112 contemplates experimentation. *See, e.g., In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Indeed, given the relatively high degree of disclosure of using two power sources (described above), it is difficult to conceive of one having ordinary skill in the art who would have been hamstrung and unable to practice the claimed invention, again bearing in mind that the specification is presumed enabling. Nevertheless, Appellants submit that the specification does “clearly teach” the disputed claim terminology of claims 1, 11, 19, and 20. At the very least, only minimal experimentation may be needed.

Appellant would again refer to page 3 of the specification where it is described that use of a down-converting circuit increases power consumption. In order to overcome this problem, the

LSI system, as illustrated in Fig. 17, the use of two external power supply sources to generate external power supply voltages VDDH and VDDL has been employed. These independently generated power supply voltages are used in the embodiments described throughout the Application, as we have described above. Thus, the written description does “clearly teach” that “two power sources, the external power supply voltage VDDH for DRAM and the power supply voltage VDDL for logic, are used.” (*See, page 3, lines 17-19*).

Armed with this knowledge, one of ordinary skill in the art reviewing the embodiments disclosed in the application would readily understand that each power-on detector 11, 12 detects power-on of a respective independent power supply received. This is clearly illustrated by at least Fig. 1 and the corresponding timing diagrams of Figs. 4 and 5.

In Section 11, on page 7, of the Final Office Action, the Examiner states even further that “it has been known in the art that a power supply voltage can be generated by another power supply voltage by using a voltage step down circuit or a voltage boosting circuit.” However, the written description of the specification discredits use of a voltage step down circuit because “[w]hen the logic power supply voltage VDDL is generated by down-converting the external power supply voltage VDDH for DRAM, an ineffective power in a down-converting circuit is increased to increase power consumption.” (*See specification, page 4, lines 6-10*). The written description of the specification accordingly describes the use of “two power sources, the external power supply voltage VDDH for DRAM and the power supply voltage VDDL for logic” to overcome problems inherent to down-conversion. (*See specification, page 3, lines 17-19*). It is this structure in which the claimed subject matter is based, and problems with the use to two sources which the present invention intends to overcome.

The Examiner has not made it clear why one of skill in the art when practicing the present invention would use a voltage step down circuit for generating two power supply voltages when the written description explicitly states and describes undesirable affects of using voltage converting circuitry in this manner. To conclude otherwise would be to presume one skilled in the art would not be able to comprehend what is explicitly stated in the Application. Appellants are aware of no such legal presumption. Indeed, it is difficult to envision anyone having ordinary skill in the art, given the guidance of the present disclosure, would not understand and comprehend to provide two power supply sources which, in turn, enables independent detection of power on levels according to each power supply source.

Appellants, therefore, submit that the imposed rejection of claims 1 through 24 under the first paragraph of 35 U.S.C. § 112, for lack of enabling support is not legally viable.

**B. The rejection of claims 1 through 24 under second paragraph of 35 U.S.C. § 112**

Under the grounds of rejection, the Examiner asserts that the specification fails to show the second power on detection circuit performing detection of the power on independently of the voltage level of the first power supply voltage, and the specification fails to show the first power on detection circuit performing detection of the power on independently of the voltage level of the second power supply voltage. The Examiner further contends that it is not seen where the specification teaches that there is no influence of power supply voltage VDDH on power-on detection circuit, and no influence of power supply voltage VDDL on power-on detection circuit 11.

Indefiniteness under the second paragraph of 35 U.S.C. § 112 is a **question of law**, not form. *Personalized Media Communications LLC v. U.S. International Trade Commission*, 161 F.3d 696, 48 USPQ2d 1880 (Fed. Cir. 1998); *Tillotson, Ltd v. Wlaboro Corp.*, 831 F.2d 1033, 4

*USPQ2d 1450 (Fed. Cir. 1987); Orthokinetics Inc. v. Safety Travel Chairs Inc.*, 806 F.2d 1565, 1 USPQ2d 1081 (Fed. Cir. 1986). Accordingly, in rejecting a claim under the second paragraph of 35 U.S.C. § 112, the Examiner must provide a basis in fact and/or cogent technical reasoning to support the ultimate legal conclusion that one having ordinary skill in the art, with the supporting specification in hand, would not be able to reasonably ascertain the scope of protection defined by a claim. *In re Okuzawa*, 537 F.2d 545, 190 USPQ 464 (CCPA 1976). Significantly, consistent judicial precedents holds that reasonable precision in light of the particular subject matter involved is all that is required by the second paragraph of 35 U.S.C. § 112. *Zoltek Corp. v. United States*, 48 Fed. Cl. 240, 57 USPQ2d 1257 (Fed. Cl. 2000); *Miles Laboratories, Inc. v. Shandon, Inc.*, 997 F.2d 870, 27 USPQ2d 1123 (Fed. Cir. 1993); *North American Vaccine, Inc. v. American Cyanamid Co.*, 7 F.3d 1571, 28 USPQ2d 1333 (Fed. Cir. 1993); *U.S. v. Teletronics Inc.*, *supra*; *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ (Fed. Cir. 1986). Appellant would stress that claims must be interpreted as one having ordinary skill in the art would have interpreted the claims in light of and consistent with the supporting specification. *Zoltek Corp. v. United States*, *supra*; *Miles Laboratories, Inc. v. Shandon, Inc.* *supra*.

As described above there is clear support for the claim language at issue. Namely, it has been described in the written description that two external power supply sources supply power supply voltages VDDH and VDDL, which are received by power on detection circuit 10 and power on detection circuit 11, respectively. Then, as described above, each power-on detector 10, 11 outputs a signal in accordance with detection of power-on of the corresponding power supply voltage. Because separate power-on detection circuitry 10, 11 receive independent voltages VDDL, VDDH, respectively, it is most certainly clearly disclosed that there is no influence of one power on detection circuit on the other.

Appellants, therefore, submit that the imposed rejection of claims 1 through 24 under the first paragraph of 35 U.S.C. § 112, for indefiniteness is not legally viable.

**C. Claims 1-3, 7, 19, 21 and 23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Crotty**

In rejecting the above-identified claims as being anticipated by Crotty, the Examiner does not consider certain limitations of independent claims 1 and 19. More particularly, the Examiner alleges that the specification fails to teach elements recited under the enablement rejection, discussed above, and therefore “the limitation “independently” of the voltage level of the first or second power supply voltage is not given any patentable weight.” (*See Final Office Action, Section 7*). The Examiner further alleges that Crotty identically discloses the other elements of the claims 1 and 19. (*See id.*). The Examiner’s position is not legally viable, and even if so, Crotty fails to identically teach each and every element of claims 1 and 19.

The factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized position of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003); *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002). Moreover, in imposing a rejection under 35 U.S.C. §102 for lack of novelty, the Examiner is charged with the burden of specifically identifying where an applied reference discloses each and every feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).

That burden has not been discharged. It is not apparent and the Examiner has failed to specifically identify where Crotty discloses or suggests a semiconductor device including

detectors for *independently performing detection*. This is not a matter of interpreting claims broadly. This is a matter of the Examiner choosing to ignore express claim limitations, *i.e.*, as the Examiner states “the limitation ‘independently’ of the voltage level of the first or second power supply voltage is not given any patentable weight.” (*See Final Office Action, Section 7, paragraph 2*). The Examiner has failed to meet his burden for lack of novelty (explicitly acknowledged by the Examiner) by specifically identifying where an applied reference discloses each and every feature of a claimed invention. There is no known legal precedent permitting an Examiner to ignore claim limitations just because he believes that the claim limitations are not supported by the written description.

There are significant fundamental differences between the claimed inventions and the device disclosed by Crotty that undermines the Examiner’s factual determination that Crotty discloses a semiconductor device identically corresponding to that claimed. These fundamental differences are discussed further below.

Contrary to the teachings of Crotty, claims 1 and 19 require detecting power-on (or a voltage level) independently of another voltage level. Portions of claims 1 and 19 have been reproduced again (*See supra, Section VIII(A)*) for the Examiner’s convenient reference.

Claim 1 recites “a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage *independently of a voltage level of said first power supply voltage*, to activate a second power-on detection signal according to a result of detection, *said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage.*”

Similar language relating to *independently performing detection* can be found in claims 19 as well, reproduced below. Claim 19 recites “each power-up detection circuit detecting a

voltage level of a corresponding power supply voltage *independently of a voltage level of the power supply voltage other than the corresponding power supply voltage.*"

Crotty does not disclose the elements recited above. Crotty discloses in Fig. 6 a power-on detection circuit including dual voltage detection circuit 210 for generating a first voltage level detection signal VD1 having a voltage level determined according to the first power supply voltage Vcc1 *only* when the second power supply voltage Vcc2 is in a steady state. (*Emphasis Added*). This is because the voltage detection signal VD1 is driven by circuitry powered by the second power supply Vcc2, and therefore, must be at a steady state to generate the first voltage level detection signal VD1. (*See Crotty, col. 2, lines 45-55*). A second voltage level detection circuit 630 detects a voltage level of the second power supply voltage Vcc2 to generate the second voltage level detection signal VD2. A buffer circuit 650 receiving signals POR1, POR2 corresponding to VD1 and VD2, respectively, generates the power-on detection signal POR in accordance with voltage level detection signals VD1 and VD2. Consequently, when the second power supply voltage Vcc2 is not supplied (or is at a level below adequate), the first and second power-on detection signals POR1 and POR2 are in an inactive state. (*See col. 9, lines 5-15 and lines 18-24*). Thus, the power-on detection signal POR is also in an inactive state.

In Crotty, detection of Vcc1, the first power supply voltage, is completely dependent on a second power supply voltage, Vcc2. To do otherwise would be contrary to the intended purpose of Crotty because Crotty teaches a dual voltage detector 210 for detecting Vcc1 dependent on a steady level of Vcc2 (*See Crotty, col. 2, lines 45-55*) to overcome the problems of "erroneous results" when a "circuit is partly power up." (*See col. lines 24-31*).

Accordingly, Crotty fails to identically teach "a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply

voltage *independently of a voltage level of said first power supply voltage*, to activate a second power-on detection signal according to a result of detection, *said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage*,” as claim 1 recites; and fails to identically teach “each power-up detection circuit detecting a voltage level of a corresponding power supply voltage *independently of a voltage level of the power supply voltage other than the corresponding power supply voltage*,” as claim 19 recites.

Claim 1 further recites “a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.”

Claim 19 further recites “a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.”

As regards the “main power-on detection circuit,” the Examiner takes the position that “active” [and “inactive”] are considered the states of a signal... a low state is seen as active state, and a high state is seen as inactive state.” (*See Office Action of 03/25/2003, Section 12*). The Examiner states further “[o]ne can define a level of a signal as an ‘active state’ or inactive state depending on his or her preference.” Because the written description of the specification describes a low level signal as an active state, the Examiner states that “a low level of the Power-

On Reset signal (POR1, POR2) [of Crotty] is interpreted as an active state..." (See *Final Office Action*, Section 11). The Examiner interprets the claims in this manner so that Crotty reads on the main power-on detection circuit elements of claims 1 and 19.

More particularly, the Examiner takes this position because buffer circuit 650 (which the Examiner correlates is the claimed main power-on detection circuit) may be an AND gate, and asserts that the AND gate, *while not considering any other factors*, could output a main power-on detection signal in accordance with the claims. This interpretation is contrary to the operation of the actual buffer circuit 650 disclosed by Crotty. On col. 9, lines 20-24, Crotty explicitly states that "[buffer] circuit 650 outputs a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period time." Therefore, in order to employ an AND gate as the buffer, an active state of a Power-On Reset signal (POR1, POR2) must be a high state (and not a low state as asserted by the Examiner) to follow disclosed implementation of the buffer circuit 650. In other words, when any of the supply voltages are less than adequate (supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2), the POR signal must be in a power-off logic level. This output state for an AND gate corresponds to inputs of (0,0), (0,1) and (1,0). To state it another way, when the voltage level of the first power supply voltage Vcc1 is insufficient, the internal circuit receiving the second power supply voltage for operation is reset. Therefore, Crotty is directed to detection of a single power application sequence. Specifically, when the first power supply voltage is applied while the second power supply voltage is not applied, the power on reset signal POR is activated, as shown in Figs. 3(b), 3(d), and Fig. 8 of Crotty.

Following the Examiner's interpretation of Crotty, to employ a power-on reset signal,

rendered active from activation of a first activated power-on detection signal (inputs to AND gate of (1,0) or (1, 0)) of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals (inputs to the AND gate of (0, 0)), would be contrary to the explicit teachings of Crotty using an AND gate as a buffer. In other words, following the Examiner's interpretation, buffer circuit 650 would be incapable of outputting "a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period time," as Crotty requires.

In accordance with the foregoing, Crotty fails to identically disclose each and every element of independent claims 1 and 19. Claims dependent therefrom are patentable at least based on dependency to any one of these claims. Accordingly, the rejection of claims 1-3, 7, 19, 21 and 23 under 35 U.S.C. §102(e) maintained by the Examiner should be withdrawn.

**D. Claims 11, 16-18, 20, 22 and 24 stand rejected under 35 U.S.C. §103(a) as being obvious over Crotty.**

In rejecting the above-identified claims as being obvious over Crotty, the Examiner does not consider certain limitations of independent claims 1 and 20, as in the case of the anticipation rejection discussed above. While the Examiner's position is not legally erroneous, the Crotty combination fails to identically teach each and every element of claims 11 and 20. Appellants submit that the record does not establish obviousness for any of the claims on appeal when considered within the framework of well developed legal precedent, briefly summarized below.

Obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art, *Graham v. John Deere Co.* 383 U.S. 1, 13, 148 USPQ 459, 465 (1966). In making this determination, the PTO is charged

with the initial burden of identifying a source in the applied prior art for: (1) claim features; and (2) the realistic requisite motivation for combining applied references to arrive at the claimed invention with a reasonable expectation of successfully achieving a specific benefit. *Smith Industries Medical Systems v. Vital Signs*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999). Even if the prior art *could* have been modified so as to result in the combination defined by the claims, the modification would not have been obvious unless the prior art suggested the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using appellant's claims as a guide. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). A compelling reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention must be formulated. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Rejections under 35 U.S.C. §103 must be predicated upon facts, not assumptions. *In re Freed*, 425 F.2d 785, 165 USPQ 570 (CCPA 1970); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967); *In re Lunsford*, 357 F.2d 385, 148 USPQ 721 (CCPA 1966). What may or may not be known in general does not establish the requisite realistic motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995). The requisite motivation is not an abstract concept, but must stem from the applied prior art as a whole and have realistically impelled one having ordinary

skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). In consideration of the prior art as a whole, it is impermissible to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *In re Wesslau*, 353 F.2d 241, 147 USPQ 393. The totality of the prior art disclosures must not lead substantially away from the claimed invention. *In re Hedges*, 753 F.2d 781, 228 USPQ2d 685 (Fed. Cir. 1986). Emphasis in a reference of the importance of a feature is a significant factor in determining whether or not it would have been obvious to change the disclosed feature. *In re Bell*, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993).

Adverting to the claims, claim 11 recites "a power-on detection circuit for detecting power-on of a second power supply voltage *independently of a voltage level of said internal voltage*, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage *independently of a voltage level of the second power supply voltage*."

Also, claim 20 recites "power-on detection circuitry..., for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage *independently of the voltage level of said at least one internal voltage*..., said internal voltage power-up detection circuitry performing detection *independently of the voltage level of the at least one power source voltage*."

Repeatedly throughout the Examiner's analysis, the limitations italicized above have been completely ignored, as in the case with the anticipation rejection. In the case of an obviousness

rejection, the Examiner is charged with the initial burden of identifying each and every element in a combination and must provide proper motivation for the combination. By the Examiner choosing to ignore claim limitations that are *italicized* above, the Examiner has failed to discharge this initial burden. Appellants are unaware of any case law precedent which lowers the Examiner's burden of proof for an obviousness rejection when the indefiniteness and lack of support is also alleged.

As in claims 11 and 20, there are significant fundamental differences between the claimed inventions and the device disclosed by Crotty that undermines the Examiner's factual determination that the Crotty combination discloses a semiconductor device identically corresponding to that claimed. These fundamental differences have been discussed above under the anticipation rejection analysis relating to the language found italicized in the claims above, and detailed arguments on this point are not repeated for sake of conciseness.

In summary, Crotty fails to disclose *independent detection* as is required by claim 11 and by claim 20. Crotty also fails to disclose main power detection circuitry (claim 11) or power-on detection circuitry (claim 20).

Specifically, in claim 11, the "main power-on detection signal [is] rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal." Because the signal is "rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal," the buffer circuit 650 of Crotty would be incapable of outputting "a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for

longer than a transient period time,” as is required.

In claim 20, the “main power-on detection signal [is] made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.” Because the signal is “made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal,” the buffer circuit 650 of Crotty would be incapable of outputting “a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate or if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period time,” as is required.

Other issues are apparent in the Examiner’s obviousness analysis are discussed further below.

The Examiner alleges that Fig. 9 of Crotty discloses all of the limitations of claims 11 and 20 except for the internal voltage generation circuit receiving a first power supply and generating an internal voltage.

Col. 9 of Crotty, as the Examiner references, describes the embodiment incorporating voltage detection circuit 630 in parallel with dual-voltage detection circuit 210 of Fig. 2, the output of which is received by a dual-input low pass filter 930. The filter includes an OR gate 950 for removing transient signal levels that the Examiner considers to be analogous with the disclose main power detection circuitry (claim 11) or power-on detection circuitry (claim 20). However, it is buffer circuit 650 of Crotty which outputs the main power signal, and has been distinguished above.

Also, in the Office Action of November 7, 2002, the Examiner acknowledged that Crotty does not disclose internal voltage generation circuits of 11 and 20, but asserts that it would have been obvious to use a voltage step-down circuit. Specifically, the Examiner states that it is well known in the arts that 5 volts is a common voltage level. Because Crotty teaches using 3.3 volts, the Examiner asserts that it would be obvious to use a step down circuit for down-converting a supplied voltage.

On page 13 of the Amendment dated February 7, 2003, Applicants traversed and pointed out to the Examiner that a conclusion of obviousness must be factually supported, evidence must be produced to support such a modification, and motivation must be provided. In the Office Action of March 23, 2003, and in response thereto, the Examiner simply states that "it is notorious well known in the art that a voltage step down circuit is [used]..." However, simply stating that something is "notoriously" well-known does not rise to the level of factual support of a modification. Applicants again seasonably traversed the Examiner's assertion that combination is notoriously well-known in the art, requested that the Examiner produce evidence thereof, and submit proper motivation, as previously requested. In the Final Office Action of August 20, 2003, the Examiner reiterated that use of a voltage step-down circuit is notoriously well known, and but in the responsive arguments (*See Section 11*), U.S. Patent No. 5,457,421 (the '421 patent) has been referenced as one example of a voltage step-down circuit.

However, Appellants again emphasize that motivation must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Simply stating that the '421 patent shows an example of

the voltage step-down circuit without providing some type of motivation gleaned from the references as a whole to modify the invention is not legally viable, and equates to what is generally referred to as “piecemeal examination.” Notwithstanding, the Examiner has failed to meet his burden of proof.

In accordance with the foregoing, Crotty fails to identically disclose each and every element of independent claims 11 and 20. Claims dependent therefrom are patentable at least based on dependency to any one of these claims. Accordingly, the rejection of claims 11, 16-18, 20, 22 and 24 under 35 U.S.C. §103 maintained by the Examiner should be withdrawn.

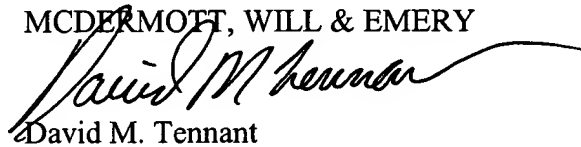
### **IX. CONCLUSION**

Based upon the argument submitted *supra*, Appellants submit that the imposed rejections under the first and second paragraphs of 35 U.S.C. §112 and under 35 U.S.C. §§102 and 103 are erroneous. Appellants, therefore, solicit the Honorable Board to reverse each of the Examiner’s rejections of the appealed claims under the first and second paragraphs of 35 U.S.C. §112 and under 35 U.S.C. §§102 and 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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## X. APPENDIX

1. (Previously Presented) A semiconductor integrated circuit device comprising:
  - a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;
  - a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage independently of a voltage level of said first power supply voltage, to activate a second power-on detection signal according to a result of detection, said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage;
  - a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.
2. (Original) The semiconductor integrated circuit device according to claim 1, wherein said main power-on detection circuit comprises
  - a first reset element responsive to activation of said first power-on detection signal for resetting a first node to a first voltage level,
  - a second reset element responsive to activation of said second power-on detection signal for resetting said first node to said first voltage level, and

a circuit coupled to said first node and receiving said first power supply voltage as an operation power supply voltage for inactivating said main power-on detection signal and setting said first node to a second voltage level when both of said first and second power-on detection signals are inactivated.

3. (Original) The semiconductor integrated circuit device according to claim 1, further comprising a converting voltage application detection circuit receiving a voltage different in voltage level from said second power supply voltage as an operation power supply voltage for converting a voltage level of said main power-on detection signal to generate a converted voltage application detection signal.

4. (Original) The semiconductor integrated circuit device according to claim 1, further comprising:

an internal voltage generation circuit for generating an internal voltage from said first power supply voltage, said internal voltage differing in voltage level from said second power supply voltage; and

an internal circuit reset when said main power-on detection signal is activated, and activated, when said main power-on detection signal is inactivated, for converting a signal having an amplitude of said second power supply voltage level into a signal having an amplitude of the internal voltage level.

5. (Original) The semiconductor integrated circuit device according to claim 4, wherein said internal voltage is a boosted voltage higher in voltage level than said first power

supply voltage.

6. (Original) The semiconductor integrated circuit device according to claim 4, wherein said internal voltage is a down-converted voltage lower in voltage level than said first power supply voltage.

7. (Original) The semiconductor integrated circuit device according to claim 1, wherein the first and second power supply voltages are applied to a storage device and said second power supply voltage is applied to a logic circuit, the storage device and the logic circuit being integrated on a common semiconductor chip.

8. (Original) The semiconductor integrated circuit device according to claim 1, wherein said main power-on detection signal has an amplitude of the first power supply voltage level, and

said semiconductor integrated circuit device further comprises:

an internal voltage generation circuit for generating, from said first power supply voltage, an internal voltage different in voltage level from said second power supply voltage;

an internal signal generation circuit for generating an internal signal having an amplitude of the internal voltage level from a signal having an amplitude of the second power supply voltage level, said internal signal generation circuit including a buffer circuit receiving said internal voltage as an operation power supply voltage for generating said internal signal; and

a converting voltage application detection circuit for converting said main power-on detection signal into a converted voltage application detection signal having an amplitude of said

internal voltage level and applying the converted voltage application detection signal to said buffer circuit, said buffer circuit being reset when said converted voltage application detection signal is activated.

9. (Original) The semiconductor integrated circuit device according to claim 8, wherein said internal voltage generation circuit includes a boosting circuit for boosting said first power supply voltage to generate said internal voltage.

10. (Original) The semiconductor integrated circuit device according to claim 8, wherein said internal voltage generation circuit includes an internal down-converting circuit for down-converting said first power supply voltage to generate an internal power supply voltage as said internal voltage.

11. (Previously Presented) A semiconductor integrated circuit device comprising;  
an internal voltage generation circuit receiving a first power supply voltage and generating, from said first power supply voltage, an internal voltage different in voltage level from said first power supply voltage;

an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage independently of a voltage level of said internal voltage, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage independently of a voltage level of the

second power supply voltage; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal.

12. (Original) The semiconductor integrated circuit device according to claim 11, further comprising an internal signal generation circuit inactivated when the main power-on detection signal from said main power-on detection circuit is activated, and activated, when said main power-on detection signal is inactivated, for generating an internal signal having an amplitude of said internal voltage level from a signal having an amplitude of said second power supply voltage level.

13. (Original) The semiconductor integrated circuit device according to claim 12, wherein

said internal signal generation circuit includes a buffer circuit receiving said internal voltage as an operation power supply voltage and generating said internal signal, said buffer circuit being reset when said main power-on detection signal is activated and buffering a level converted signal to generate said internal signal when said main power-on detection signal is inactivated.

14. (Original) The semiconductor integrated circuit device according to claim 11, wherein said main power-on detection signal is a signal having an amplitude of said internal voltage level, and

said integrated circuit device further comprises

a level conversion circuit for converting a voltage level of said main power-on detection signal to generate a converted voltage application detection signal, and

an internal signal generation circuit inactivated when said converted voltage application detection signal is activated and activated, when said converted voltage application detection signal is inactivated, for converting a level of a signal having an amplitude of said second power supply voltage level to generate an internal signal having an amplitude equal to an amplitude of said converted voltage application detection signal.

15. (Original) The semiconductor integrated circuit device according to claim 14, further comprising an internal power supply circuit for generating, from said first power supply voltage, an internal power supply voltage different in voltage level from said internal voltage, wherein

said internal signal generation circuit includes a buffer circuit receiving said internal power supply voltage as an operation power supply voltage and buffering a level converted signal for outputting, said buffer circuit having an internal node being reset when said converted voltage application detection signal is activated.

16. (Original) The semiconductor integrated circuit device according to claim 11, wherein said internal voltage generation circuit includes a boosting circuit for boosting said first

power supply voltage.

17. (Original) The semiconductor integrated circuit device according to claim 11, wherein said internal voltage generation circuit includes a down-converting circuit for down-converting said first power supply voltage to generate said first internal voltage.

18. (Original) The semiconductor integrated circuit device according to claim 11, wherein the first and second power supply voltages are applied to a storage device and said second power supply voltage is applied to a logic circuit, said storage device and said logic circuit being integrated on a common semiconductor chip.

19. (Previously Presented) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages, each power-up detection circuit detecting a voltage level of a corresponding power supply voltage independently of a voltage level of the power supply voltage other than the corresponding power supply voltage; and

a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

20. (Previously Presented) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltages differing in voltage level from each other;

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage independently of the voltage level of said at least one internal voltage, to generate at least one power-on detection signal for the respective at least one power source voltage, said internal voltage power-up detection circuitry performing detection independently of the voltage level of the at least one power source voltage; and

main power-on detection circuitry responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.

21. (Previously Presented) The semiconductor integrated device according to claim 1,

wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

22. (Previously Presented) The semiconductor integrated circuit device according to claim 11, wherein activation of the detection signal indicates instability of a corresponding power supply voltage, and inactivation of the detection signal indicates stability of the corresponding power supply voltage.

23. (Previously Presented) The semiconductor device according to claim 19, wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

24. (Previously Presented) The semiconductor device according to claim 20, wherein the activation of the detection signal indicates instability of a corresponding voltage and the inactivation of the detection signal indicates stability of the corresponding voltage.